WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first portion having a first substrate, a conductive layer and an insulating layer laminated on the first substrate and a bonding surface that is chemically mechanically polished and exposes a conductive region and an insulating region;

a second portion having a second substrate, a conductive layer and an insulating layer laminated on the second substrate and a bonding surface that is chemically mechanically polished and exposes at least a conductive region; and wherein

the bonding surface of the first portion and the bonding surface of the second portion are solid-state-bonded to each other and

at least one of the bonding surface of the first portion and the bonding surface of the second portion has the insulating region lowered with respect to the conductive region.

2. A semiconductor device as claimed in claim 1, wherein dishing portions of the conductive regions are bonded to each other.

3. A semiconductor device as claimed in claim 1, wherein the conductive region of the first portion and the conductive region of the second portion are solid-state-

bonded to each other, and the insulating region of the first portion and the insulating region of the second portion face each other with interposition of a clearance.

4. A semiconductor device as claimed in claim 3, wherein the insulating region that surrounds the conductive region of the first portion and the insulating region that surrounds the conductive region of the second portion face each other with interposition of a clearance.

5. A semiconductor device as claimed in claim 1, wherein the conductive region of the first portion and the conductive region of the second portion are solid-state-bonded to each other, and the insulating region of the first portion and the insulating region of the second portion are put in contact with or solid-state-bonded to each other.

6. A semiconductor device as claimed in claim 5, wherein the insulating region that surrounds the conductive region of the first portion and the insulating region that surrounds the conductive region of the second portion are put in contact with or solid-state-bonded to each other.

7. A semiconductor device as claimed in claim 4, wherein the conductive regions are end surfaces of through hole conductors and the insulating regions are end surfaces of through hole insulators that surround the respective through hole conductors.

8. A semiconductor device as claimed in claim 6, wherein the conductive regions are end surfaces of through hole conductors and the insulating regions are end surfaces of through hole insulators that surround the respective through hole conductors.

9. A semiconductor device as claimed in claim 1, wherein the first substrate or the second substrate is any one of a semiconductor substrate, an inorganic substrate and an organic substrate.

10. A semiconductor device fabricating method comprising the steps of:

forming a first portion having a first substrate, a conductive layer and an insulating layer laminated on the first substrate and a bonding surface that is chemically mechanically polished and exposes a conductive region and an insulating region;

forming a second portion having a second substrate, a conductive layer and an insulating layer laminated on the second substrate and a bonding surface that is chemically mechanically polished and exposes at least a conductive region;

selectively etching the insulating region of at least one of the bonding surface of the first portion and the bonding surface of the second portion, thereby lowering

the surface of the insulating region with respect to the surface of the conductive region; and

applying pressure welding loads to the first portion and the second portion for achievement of solid state bonding of the bonding surface of the first portion to the bonding surface of the second portion and for achievement of electrical connection of the conductive region of the first portion with the conductive region of the second portion.

11. A semiconductor device fabricating method as claimed in claim 10, wherein the surface of the insulating region is lowered by reactive ion etching.

12. A semiconductor device fabricating method as claimed in claim 10, wherein etching is performed so that a height of a bottom of a dishing portion of the conductive region and a height of the insulating region become approximately equal to each other.

13. A semiconductor device fabricating method as claimed in claim 10, wherein the conductive region of the first portion and the conductive region of the second portion are solid-state-bonded to each other, and the insulating region of the first portion and the insulating region of the second portion face each other with interposition of a clearance.

14. A semiconductor device fabricating method as claimed in claim 13, wherein the insulating region that surrounds the conductive region of the first portion and the insulating region that surrounds the conductive region of the second portion face each other with interposition of a clearance.

15. A semiconductor device fabricating method as claimed in claim 10, wherein the conductive region of the first portion and the conductive region of the second portion are solid-state-bonded to each other, and the insulating region of the first portion and the insulating region of the second portion are put in contact with or solid-state-bonded to each other.

16. A semiconductor device fabricating method as claimed in claim 15, wherein the insulating region that surrounds the conductive region of the first portion and the insulating region that surrounds the conductive region of the second portion are put in contact with or solid-state-bonded to each other.

17. A semiconductor device fabricating method as claimed in claim 14, wherein the conductive regions are end surfaces of through hole conductors and the insulating regions are end surfaces of through hole insulators that surround the respective through hole conductors.

18. A semiconductor device fabricating method as claimed in claim 16, wherein the conductive regions are end surfaces of through hole conductors and the insulating regions are end surfaces of through hole insulators that surround the respective through hole conductors.

19. A semiconductor device fabricating method as claimed in claim 10, wherein the first substrate or the second substrate is any one of a semiconductor substrate, an inorganic substrate and an organic substrate.